TABLE I
THE CHARACTERISTIC IMPEDANCE OF THE POLYGONAL LINE WITH CIRCULAR INNER CONDUCTOR

	shape (a) N=3			shape (b) N=4			
r_b/r_c	present work	Seshadri and Rajaian[6]	Lin[8]	present work	Seshadri and Rajaian[6]	Lin[8]	Riblet[3]
0.05	186.46	187.32	185.16	184.14	184.42	183.77	
0.1	144.90	145.70	144.36	142.59	142.50	142.21	
0.2	103.32	104.08	102.05	101.02	101.18	100.66	
0.3	78.97	79.74	77.74	76.69	76.84	76.35	
0.4	61.66	62.45	60.49	59.42	59.56	59.10	
0.5	48.20	49.03	47.12	46.00	46.16	45.73	46.09
0.6	37.13	38.01	36.19	35.00	35.20	34.80	35.15
0.7	27.67	26.57*	26.94	25.66	25.89	25.55	25.85
0.8	19.30	20.14	18.94	17.46	17.71	17.55	17.68
0.9	11.47	12.06	11.88	9.97	10.15	10.49	10.13
0.95	7.34		8.64	6.20		7.25	6.25
0.99	3.02		6.17				
0.998	1.24		5.68	1.07		4.29	1.00

	shape (c) N=5			shape (d) N=6		
r_b/r_c	present work	Seshagiri [1]	Lin[8]	present work	Seshagiri [1]	Lin[8]
0.05	182.67	182.58	182.94	181.82	181.64	182.38
0.1	141.12	140.92	141.38	140.26	140.01	140.82
0.2	99.52	99.26	99.83	98.71	98.38	99.27
0.3	75.26	74.91	75.52	74.39	74.04	74.96
0.4	57.98	57.65	58.27	57.14	56.79	57.71
0.5	44.58	44.30	44.89	43.75	43.43	44.34
0.6	33.62	33.42	33.97	32.80	32.58	33.41
0.7	24.32	24.24	24.72	23.53	23.34	24.16
0.8	16.22	16.26	16.72	15.47	15.37	16.16
0.9	8.93	9.06	9.66	8.27	8.25	9.10
0.94	6.09	6.23	7.05	5.53	5.52	6.49
0.99	2.04		3.94	1.76		3.39

* It should read 28.57

TABLE II
THE CHARACTERISTIC IMPEDANCE OF THE SHAPES (e)–(g)

	shape (e) parallel plates			shape (f) trough (b=2h)		shape (g) rectangle (a=2b)		
2r/b	present work	Wheeler [1]	Lin [1]	present work	Chisholm [1]	present work	Lin and Chuang[1]	Pan [9]
0.05	194.07			188.90	188.89	193.64	193.64	193.64
0.1	152.49	152.54	152.53	147.34	147.33	152.07	152.06	152.13
0.2	110.85	110.98	110.97	105.74	105.74	110.43	110.52	110.56
0.3	86.39	86.63	86.64	81.37	81.36	85.98	86.19	86.15
0.4	68.92	69.29	69.34	64.81	64.81	68.51	68.89	68.72
0.5	55.21	55.72	55.84	50.48	50.46	54.82	55.39	55.07
0.6	43.88	44.42	44.65	39.32	39.28	43.44	44.21	43.72
0.7	33.86	34.52	34.91	29.72	29.67	33.53	34.48	33.86
0.8	24.75	25.35	25.93	21.13	21.12	24.46	25.52	24.82
0.9	15.68	16.03	16.78	12.91	13.24	15.46	16.44	15.73
0.94				9.40	10.19			
0.95	10.49	10.58	11.37			10.32	11.11	10.46
0.99	4.49	4.17	4.92	3.53		4.41	4.80	4.39

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A Simplified Large-Signal Simulation of a Lumped Element TEO Based on a Phase Plane Technique

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***Abstract*—The transferred electron device (TED) lumped circuit interaction is modeled by a phase plane technique. The results from this large-signal simulation are compared to those from a time-domain simulation based on the electron transport equations and are shown to be in good agreement. Results from the simulations are used as the design specifications for a *J*-band MIC TEO with excellent results indicating the potential of this CAD technique.**

I. INTRODUCTION

The microwave performance characteristics and frequency of operation of a transferred electron device (TED) are dependent not only on the physical parameters of the TED but also on the external circuit in which the device is embedded. Several studies [1]–[3] have attempted to simplify the characterization of this highly nonlinear device–circuit interaction. Simple analysis yields some understanding of the TED behavior but has been of little direct use to the design engineer who has relied mainly on indirect measurements [4]–[6] of the admittance of a particular diode at a specific frequency of operation, to optimize performance. Only in the case of LSA oscillator design has a simplified analysis been of any significance. In the LSA mode [7], associated with oversize n-GaAs samples, space-charge accumulation is negligable and hence an assumption that a uniform electric-field profile exists across the device allows the voltage V_D and average electron current $\bar{I}_e$ to be linked by a piecewise-linear approximation to the electron drift velocity-electric field (v-E) characteristic of n-GaAs. This assumption is, however, invalid for short, commercial TED's in which space-charge accumulation is significant.

Large-signal time-domain simulations which are based on numerical solutions of the electron transport equations, have the advantage of assuming only the physical properties of GaAs and the geometry and doping of the TED. External circuit elements and a bias can be incorporated into these numerical schemes which are run until steady-state oscillations occur when a Fourier analysis of the voltage and current waveforms yield the frequency of operation, dynamic device admittance, RF power, and dc to RF conversion efficiency. Several large-signal time domain simulations have been developed [8]–[10] to determine device performance and operation but have not been compared to experimental data. Lakshminarayana and Partain [6] have, however, produced reasonable agreement between the results of their large-signal time-domain simulation [11] and dynamic device admittance data measured from diodes embedded in Sharpless Flange mounts. These large-signal time-domain simulations have the flexibility to allow both device and circuit parameters to be readily adjusted to optimize oscillator performance. However, the simulations are not only difficult to establish but require significant CPU time for each run and also many runs are required since the TED's dynamic admittance, and hence the frequency of operation cannot be preset.

This paper describes the simplified method of solving the TED lumped circuit interaction using a phase plane method [12]. These

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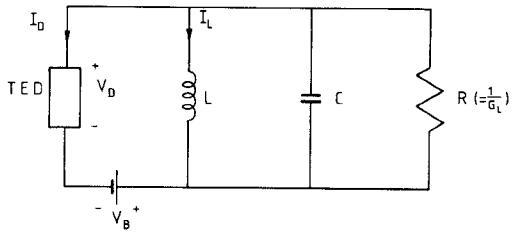


Fig. 1. TED in a parallel *LCR* circuit.

simulations are straightforward to establish and produce results in less than one second of CPU time compared to tens of minutes for a large-signal time-domain simulation. The development and accuracy of this method is centered on the modeling of the TED's dynamic $\bar{I}_e - V_D$ characteristic which is both device and circuit dependent. The phase plane method does not replace the large-signal time-domain simulation but can be used in conjunction with it to substantially reduce the CPU time used to "home in" on the circuit and device parameters required to yield optimum performance at a particular frequency or range of frequencies. Finally, the specifications for a *J*-band TEO are generated from these large-signal simulations and are realized in the form of a hybrid MIC on RT/duroid.

II. The Phase Plane Method

The TED current I_D can be represented [1] by the sum of an electron current $\bar{I}_e$ and a capacitive current $C_o dV_D/dt$ where C_o is the dielectric capacitance of the device and V_D is the terminal voltage. Thus, if the TED and lumped-element circuit with the dc bias V_B is as shown in Fig. 1, then the corresponding circuit equations are as follows:

$$L\frac{dI_L}{dt} = V_D - V_B \tag{1}$$

and

$$(C + C_0)\frac{dV_D}{dt} = -[\bar{I}_e + I_L + G_L(V_D - V_B)]. \tag{2}$$

Differentiating (2) and using (1) yields

$$\frac{d^2V_D}{dt^2} + \left(\frac{G_L + \frac{d\bar{I}_e}{dV_D}}{C + C_0}\right)\frac{dV_D}{dt} + \frac{V_D}{L(C + C_0)} = \frac{V_B}{L(C + C_0)} \tag{3}$$

which may be reduced to a first-order differential equation with the substitution $W = dV_D/dt$ yielding, with rearrangement

$$\frac{dW}{dV_D} = \frac{-\left(G_L + \frac{d\bar{I}_e}{dV_D}\right)}{C + C_0} + \frac{1}{L(C + C_0)}\left(\frac{V_B - V_D}{W}\right). \tag{4}$$

Equation (4) defines a set of integral curves on the $V_D - W$ plane which is the phase plane. In particular, the curve $dW/dV_D = 0$ defined by

$$W = \frac{V_B - V_D}{L\left(G_L + \frac{d\bar{I}_e}{dV_D}\right)} \tag{5}$$

will provide a useful visual boundary in the phase plane.

For an initial analysis the $\bar{I}_e - V_D$ characteristic is generated from an analytic fit ((1) in [13]) to the v-E characteristic of

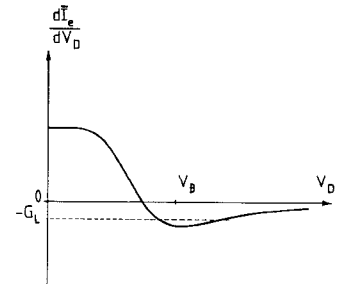
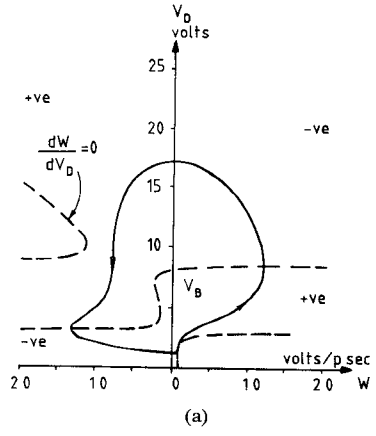
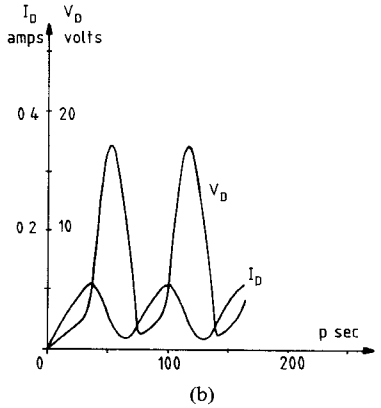


Fig. 2. $d\bar{I}_e/dV_D - V_D$ characteristic based on (6) and (1) in [13].



(a)



(b)

Fig. 3. (a) The phase plane is partitioned by the V_D-axis and $dW/dV_D = 0$. (b) Computed V_D and I_D waveforms for $C = 0$ pF, $L = 2.0$ nH, $G_L = 2$ mS, $V_B = 8$ V, $d = 8\ \mu$m, $N_D = 10^{21}$ m^{-3}, $A = 3.85.10^{-9}$ m^2.

n-GaAs. The TED voltage and electron current are given by

$$V_D = E.d \quad \text{and} \quad \bar{I}_e = A.N_D.q.v \tag{6}$$

where N_D is the doping concentration in the active region of length d and cross-sectional area A; thus, the $d\bar{I}_e/dV_D - V_D$ characteristic is as shown in Fig. 2.

A typical curve of $dW/dV_D = 0$ defined by (5) is shown in Fig. 3. By inspecting (4) zones occur where dW/dV_D is either positive or negative which leads to a cyclic trace forming the solution to (4).

The traces may be computed by a finite-difference approximation to dW/dV_D in (4) and incrementing V_D. Smooth traces may be readily produced provided care is taken to avoid the trace plots from being on or too near the $W = 0$ axis where $dW/dV_D \to \infty$. The voltage waveform may be determined from the array $V_D(N)$ and the time array $T(N)$ which may be filled at each step

of the trace computation using

$$T(N+1) = T(N) + \frac{\Delta V_D}{|W(N)|} \tag{7}$$

and since the $\bar{I}_e - V_D$ characteristic has been assumed; the device waveform $I_D(N)$ may be determined from

$$I_D(N) = \bar{I}_e(V_D(N)) + C_0 W(N). \tag{8}$$

III. $\bar{I}_e - V_D$ Characteristics

The phase plane method has been developed alongside a large-signal time-domain simulation. Using the $\bar{I}_e - V_D$ characteristic developed from (1) in [13], the phase plane produced results for the frequency of operation and RF power which were far too inaccurate to be considered useful. However, close agreement between the simulations can be achieved by using a more realistic $\bar{I}_e - V_D$ characteristic of the type shown in Fig. 4(a) which have been generated from the large-signal time-domain simulation.

Close examination of all the characteristics produced clearly showed that there is little change in their shape for increasing V_D.

The $\bar{I}_e - V_D$ characteristic developed from (1) in [13] does provide a close fit below the threshold voltage but underestimates the valley current. The characteristic can be easily modified by including parameters x and y in the analytic fit given in (9a) where T_0 is the absolute temperature of the crystal lattice ($T_0 =$ 300 K is used throughout) and E_0 is $4.10^5 \mathrm{Vm}^{-1}$

$$\bar{I}_e = AqN_D.225\frac{E}{T_0}\frac{1+\dfrac{x.0.256\left(\dfrac{E}{E_0}\right)^3}{\dfrac{T_0}{1-5.3\dfrac{T_0}{10^4}}}}{1+y.\left(\dfrac{E}{E_0}\right)^4}. \tag{9a}$$

Putting $x = 3$ and $y = 2$ has little effect on the characteristic below threshold where $E < E_0$ but, for $E > E_0$, has the effect of increasing the valley current to provide a close fit. Equation (9a) is the characteristic for increasing V_D and is curve "a" in the double-valued approximation in Fig. 5(a). Curve "b" is given by (9b) where it should be noted that $V_{\max}$ is determined

$$\frac{(V_D - V_B)^2}{(V_{\max} - V_B)^2} + \frac{(\bar{I}_e - I_V)^2}{\left[\frac{1}{2}I_v\frac{L_0}{L}\left(1 - \frac{C}{C_0}\cdot\frac{L}{L_0}\right)\right]^2} = 1 \tag{9b}$$

by the trace computation, $I_v = \bar{I}_e(V_{\max})$ and $L_0 = 1.5$ nH. Curve "c" is given by (9c), where $I_p = 150 \cdot L/L_0$ mA

$$\frac{(V_D - V_B)^2}{V_B^2} + \frac{(\bar{I}_e - I_p)^2}{\left[I_p - \frac{1}{2}I_v\frac{L_0}{L}\left(1 - \frac{C}{C_0}\cdot\frac{L}{L_0}\right)\right]^2} = 1 \tag{9c}$$

and is valid for $V_D \geq V_x$, where V_x is the voltage at the intersection between curves "a" and "c". When $V_D < V_x$, curve "a" is again used, which avoids the computations jumping to curve "a" when $dV_D/dt = 0$, causing a discontinuity of current. A further "d" is required, see Fig. 5(b), for the cases when curves "a" and "c" do not intersect, and is given by

$$\bar{I}_e = \frac{I_{\mathrm{th}}}{V_{\mathrm{th}}} \cdot V_D \tag{9d}$$

where V_{th} is an estimate of the threshold voltage (2.5 V was used for a TED with an active length of 8 μm) and $I_{\mathrm{th}} = \bar{I}_e(V_{\mathrm{th}})$ which is evaluated from (9a). Equation (9d) is valid for $V_{\mathrm{th}} < V_D < V_y$ where V_y is the intersection between curves "c" and "d".

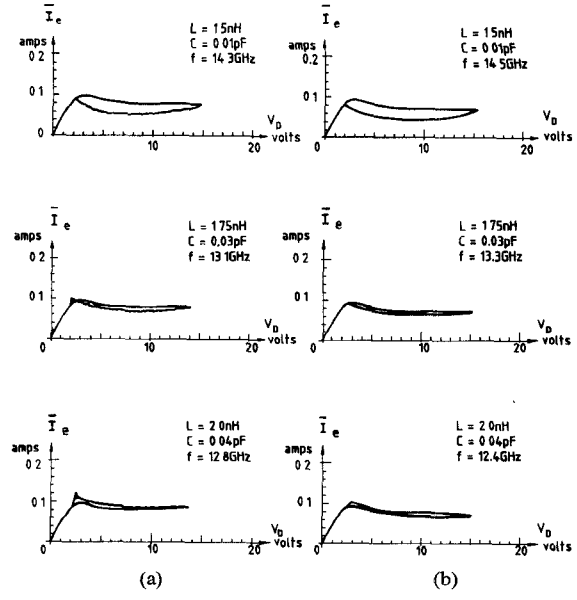


Fig. 4. $\bar{I}_e - V_D$ characteristics from (a) a large-signal time-domain simulation, and (b) the phase plane technique incorporating (9a)–(9d).

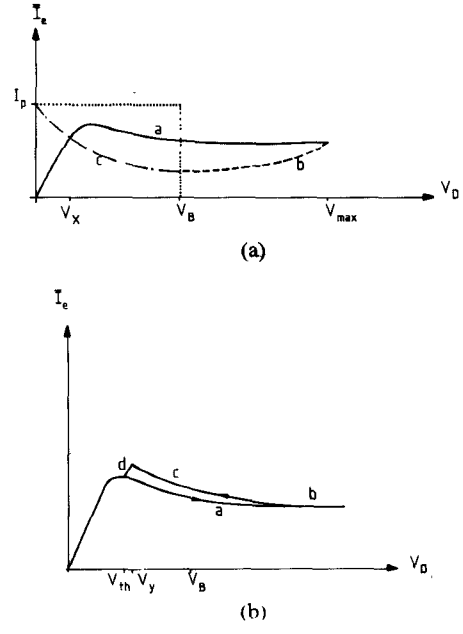


Fig. 5. Curves "a", "b", "c", and "d" defined by (9a)–(9d) provide a fit to the $\bar{I}_e - V_D$ characteristics.

The basic $\bar{I}_e - V_D$ characteristics, which are formed by (9a)–(9d), are used in the phase plane method and some results are shown in Fig. 4(b). Over the frequency range 12–15 GHz, the computed frequencies of operation were in good agreement (at best within 50 MHz, at worst within 400 MHz) to those generated by the first principle time-domain simulations and, in addition, the RF voltages were all within 0.75 V and the dc to RF conversion efficiencies within 1 percent.

IV. MIC Realization

An MIC has been fabricated on RT/Duroid 5880 by realizing the four main sections of the lumped circuit shown in Fig. 6

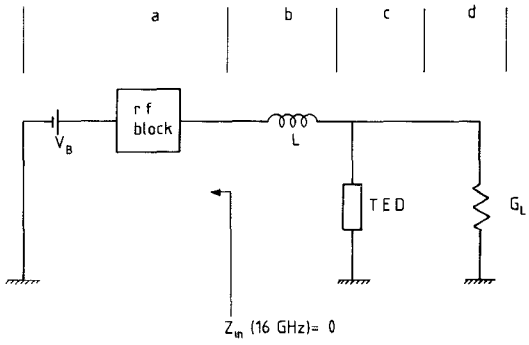


Fig. 6. The parallel *LCR* circuit, with $C = 0$, is fabricated by realizing the four main sections a–d shown

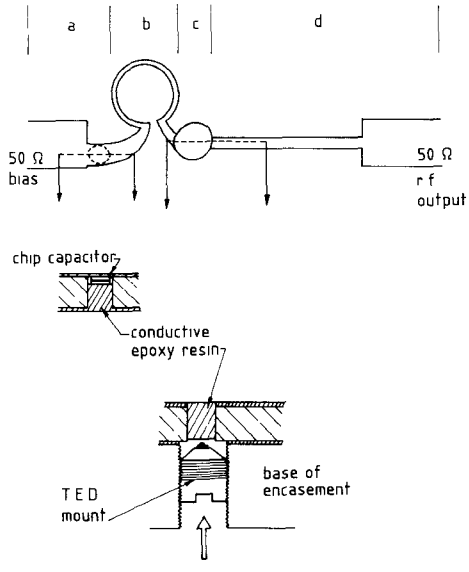


Fig. 7. Realization of the MIC on RT/Duroid.

which is equivalent to Fig. 1 with zero external circuit capacitance. The specifications, $d = 7$ μm, $N_D = 1.3.10^{21}$ m^{-3}, and $A = 4.4.10^{-9}$ m^2 of a Plessey integral heat sink TED from their batch R963, were input to the large-signal time-domain simulation and with $V_B = 8$ V, $L = 1.5$ nH, and $G_L = 2.5$ mS the predicted performance was 40 mW at 16 GHz.

The realization of the MIC is shown in Fig. 7. The loop inductor L had a track width of 70 μm and an overall diameter of 1.2 mm, the $\frac{1}{4}$ wave transformer had an impedance of 141 Ω and the RF block provided a good short circuit around 16 GHz. Particular attention was paid to producing a circuit that could be directly transferred to monolithic form; hence, bond wire connections, although much more robust than the delicate pressure contact used here, were not used and their associated parasites were avoided.

As shown in Fig. 8 the measured frequency of operation is in excellent agreement with the simulations. The measured RF power was well down on predicted values, however, several decibels of loss can be attributed to the radiation loss [14] associated with the discontinuity at the 50-Ω RF output.

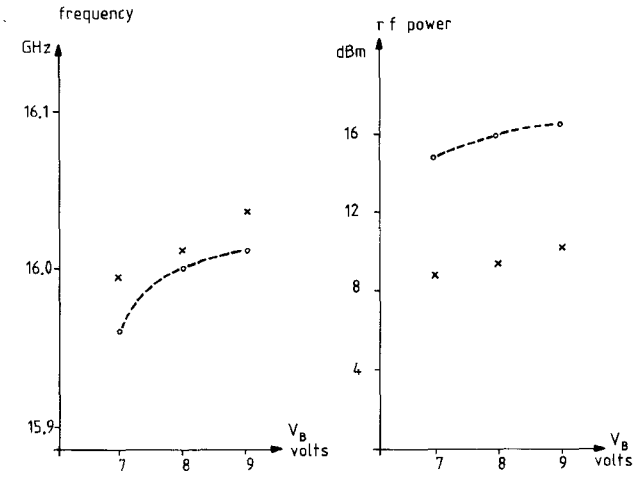


Fig. 8. Fundamental frequency of operation and RF power for several bias points (· simulated, x measured).

V. Conclusions

The phase plane method of solving the TED lumped circuit interaction has been shown to give good agreement to the results from a large-signal time-domain simulation. The method uses a double-valued $I_e - V_D$ characteristic which has been developed as a function of device and circuit parameters only. The results from the phase plane method give a good first approximation for the design specifications of a lumped element TEO. A J-band MIC TEO was fabricated on RT Duroid 5880 with a design which is directly transferable to monolithic form. The measured frequency of operation was in excellent agreement with the design specification.

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